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| 10/762,864 | 01/21/2004 | Wilson Wong | 174/295 | 5928 |

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FISH & NEAVE IP GROUP
ROPES & GRAY LLP
1211 AVENUE OF THE AMERICAS
NEW YORK, NY 10036-8704

| EXAMINER | |
|---|---|
| FOTAKIS, ARISTOCRATIS | |
| **ART UNIT** | **PAPER NUMBER** |
| 2611 | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/762,864 | WONG ET AL. | |
| | Examiner | Art Unit | |
| | Aristocratis Fotakis | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after t he mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01/21/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 - 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/21/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 7 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugiyama (US 6,396,872).

Re claims 1 and 26, Sugiyama teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Col 1, Lines 10 – 14) comprising: equalization implementation circuitry including a selectable number of taps (Fig.1); programmable circuitry for allowing a first number of taps to be specified (#25, memory circuit, Abstract, Col 19, Lines 22 – 23, Col 24, Lines 64 – 65, Fig.1); processing circuitry for computing a second number of taps (#20, Fig.1, Col 24, Lines 64 – 67 to Col 25, Lines 1 – 6); and selection circuitry for selecting one of the first and second numbers as the selectable number (#26, Fig.1, Col 25, Lines 13 – 16).

Re claim 2, Sugiyama teaches of the selection circuitry being programmable to make its selection (Col 8, Lines 33 – 35).

Re claim 3, Sugiyama teaches of the processing circuitry performing an algorithm to compute the second number (Col 19, Lines 1 – 8).

Re claim 4, Sugiyama teaches of a memory (#28, Fig.1) coupled to the processor programmable logic device circuitry coupled to the processor circuitry and the memory (Fig.1).

Re claims 5 - 6, Sugiyama teaches of a printed circuit board (Fig.1) comprising: a memory (#28, Fig.1) mounted on the printed circuit board and coupled to the programmable logic device circuitry (Fig.1).

Re claim 7, Sugiyama teaches of the printed circuit board further comprising: processor circuitry (#20, Fig.1) mounted on the printed circuit board and coupled to the programmable logic device circuitry (Fig.1).

Claims 12 – 17 and 28 - 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Debus, Jr. (US 4,773,034).

Re claims 12 and 28, Debus teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Abstract) comprising: equalization implementation circuitry (Col 2, lines 53 – 67 to Col 3, Lines 1 – 36) including at least

one selectable coefficient value (from switch #230, Fig.2); first processing circuitry (#212, Fig.2) for computing the coefficient value using a selectable starting value (Col 2, lines 53 – 67 to Col 3, Lines 1 – 12); programmable circuitry (#214, Fig.2) for allowing a first starting value to be specified (Col 3, Lines 10 – 20 and Col 7, Lines 1 - 17); second processing circuitry (#215, Fig.2) for computing a second starting value (Col 3, Lines 10 – 20 and Col 7, Lines 1 - 17); and selection circuitry (#230, Fig.2) for selecting one of the first and second starting values as the selectable starting value (Col 3, Lines 10 – 20).

Re claim 13, Debus teaches of the selection circuitry being programmable to make its selection (Col 3, Lines 10 – 20).

Re claim 14, Debus teaches of the first processing circuitry performing an algorithm to compute the coefficient value (tap-weight adjustment algorithm, Col 3, Lines 27 – 34).

Re claim 15, Debus teaches of the second processing circuitry performing an algorithm to compute the second starting value (Col 4, Lines 9 – 15).

Re claim 16, Debus teaches of a further programmable circuitry (#216, Fig.2) for allowing selection (#213) between (1) operation of the first processing circuitry to fix on the coefficient value that produces satisfactory equalization (switches going upwards

from bus #213), and (2) continued operation of the first processing circuitry to continue to possibly adapt the coefficient value even after satisfactory equalization has been produced (switches going downwards from bus #213 to receive the new coefficients from switch #230) (Col 3, Lines 12 – 16).

Re claims 17 and 29, Debus teaches of a programmable logic device circuitry for adaptively equalizing a received data signal comprising: equalization implementation circuitry including at least one selectable coefficient value; processing circuitry for computing the coefficient value (see claim 12); and programmable circuitry for allowing selection between (I) operation of the processing circuitry to fix on the coefficient value that produces satisfactory equalization, and (2) continued operation of the first processing circuitry to continue to possibly adapt the coefficient value even after satisfactory equalization has been produced (see claim 16).

Claims 22 – 23 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomisato et al (US 5,504,783).

Kokuryo teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Col 22, Lines 32 – 55) comprising: processing circuitry for computing an error signal using a selectable training pattern (Col 3, Lines 25 - 41); programmable circuitry for allowing a first training pattern to be specified (Col 22,

Lines 40 - 47); training pattern circuitry for providing a second training pattern (Col 22, Lines 47 - 54); and selection circuitry for selecting one of the first and second training patterns as the selectable training pattern (Col 23, Lines 47 - 51).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8 – 11 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (US 6,275,836) in view of Shanbhag et al (US 6,940,898) and further view of Debus.

Re claims 8 – 11 and 27, Lu teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Abstract, Fig.3) comprising: equalization implementation circuitry including taps (interpolation filter) having a selected one of integer spacing and fractional spacing relative to the symbol rate of the data signal (Abstract, Lines 1 – 13, Fig.3); processing circuitry (#74, Fig.3) for computing a (second) selection (#76a, #76b, Fig.3) between integer spacing and fractional spacing (Abstract, Lines 9 – 13, Fig.3 and Col 7, Lines 17 – 29). However, Lu does not teach of the human involvement in the invention by selecting a (first) selection of one of integer spacing and fractional spacing and a selection circuitry, for selecting one of the first and second selections as the selected one of integer spacing and fractional spacing.

Shanbhag teaches of an adaptive coefficient signal generator for adaptive signal equalizers with fractional-spaced feedback. Shanbhag in his invention discloses the advantages of the fractional spacing versus the symbol spacing as well as the

factors such as phase offset, jitter, S/N ratio sensitivity, absence or non-absence of the channel information that need to be considered in order to make a decision on what spacing parameters and type (Col 1, Lines 42 – 51, Col 2, Lines 1 – 14) are required. Therefore by considering these factors the human involvement is crucial so as to make a decision especially in initialization.

Debus teaches of the human involvement for updating the tap coefficient values (#214, Fig.2) and an algorithm for processing the tap coefficient values (#215, Fig.2) and providing a manual toggling switch (#230, Fig.2) for selecting one of the two (Fig.2, Col 3, Lines 10 – 20).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a manual programming option for selecting one of the fractional or integer spacing and a selector for selecting one of the first and second selections so as to have a system that is more user defined and controlled by the user for the case of errors made by the algorithm and having control of the system.

Re claim 11, Lu teaches of the fractional spacing is a selectable fraction of the symbol period (1/fs, sampling rate fs, Col 7, Lines 48 – 62), wherein the first selection can include a programmably specified first fraction, and wherein the second selection can include a processing-circuitry-computed second fraction (see claim rejection above).

Re claims 24 – 25 and 32, Lu, Shanbhag and Debus teach of a programmable logic device circuitry for adaptively equalizing a received data signal as discussed above in claims 8 – 11, comprising: equalization implementation circuitry having at least one sampling point with a selectable location relative to a bit period of the received signal; programmable circuitry for allowing a first location of the sampling point to be specified; processing circuitry for computing a second location of the sampling point; and selection circuitry for selecting one of the first and second locations as the selectable location. The symbol period of the tap spacings is the inverse of the sampling frequency. Changing the spacing will change the location of the sampling points.

Claims 18 – 21 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hillery (US 6,178,201) in view of Wang et al (US 6,693,958).

Re claims 18 and 30, Hillery teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Abstract) comprising: equalization implementation circuitry responsive to an error signal (Fig.1); first processing circuitry for computing a first decision directed error signal (#40, Fig.1, Col 3, Lines 54 – 67); second processing circuitry for computing a second error (#38, Fig.1, Col 3, Lines 38 – 50); and selection circuitry (#36, Fig.1) for selecting one of the first and second error signals as the error signal (Col 3, Lines 30 – 37). However, Hillery teaches of the differences between blind and non-blind adaptive equalizers (Col 1, Lines 45 – 56) but

does not specifically teach of the second processing circuitry computing the error by the use of a training pattern.

Wang teaches of an adaptive channel equalizer (#50, Fig.1) for processing a demodulated VSB signal containing terrestrial broadcast high definition television information operates adaptively in blind, training, and decision-directed modes (Abstract). When the equalizer operation is initiated, the coefficient values (filter tap weights) are usually not set at values which produce adequate compensation of channel distortions. In order to force initial convergence of the equalizer coefficients, a known "training" signal may be used as the reference signal. Training signals, eg., a pseudorandom number (PN) sequence, have been used extensively in telecommunications devices such as television receivers and telephone modems. A major benefit of employing a known PN sequence training signal in the transmission is that errors can be accurately obtained, and the equalizer can be trained to equalize the transmission channel before and during transmitting and receiving data (Col 1, lines 60 – 67 to Col 2, Lines 1 – 10).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a training sequence to compute the error for the benefit of more accurate measurements compared to computing the error without a training sequence.

Re claim 19, Hillery teaches of the selection circuitry being programmable (#34, Fig.1) to make its selection (Col 4, Lines 16 – 32).

Re claim 20, Hillery teaches of the first processing circuitry performs an algorithm (LMS) to compute the first decision directed error signal (Col 3, Lines 65 – 67).

Re claim 21, Hillery teaches of the second processing circuitry performing an algorithm (CMA) to compute the second error signal using a training pattern (Col 3, Lines 45 – 47).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER